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Silicon Integrated Low-Loss 4-Channel 5-Bit Optical True-Time Delay Lines

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Abstract: We demonstrate 4-channel tunable optical delay lines with delay > 500 ps and delay error < ±1ps. The delay loss is 3 dB/ns and the delay deviation is less than 1 ps among 4 channels.

1. Introduction

Optical true-time delay lines (OTTDLs) have been widely used in data synchronization and data processing in the optical networks. The OTTDLs realized by discrete free-space or fiber-optic components suffer from the large size, high cost, heavy weight and high power consumption. With the development of silicon photonics, silicon integrated OTTDLs have been widely studied and employed for a variety of applications such as optical buffering [1], optical time-division multiplexing (OTDM) [2, 3], and optical beamforming networks (OBFNs) [4-8], due to their compact size, low cost, light weight and low power consumption. There are several approaches to realize OTTDLs. One is to change the optical path by using switches. This method features a large delay tuning range, a low temperature sensitivity and a wide operation bandwidth. The delay can be tuned discretely and the delay deviation from the target can be well controlled by the waveguide design. Another method is to use resonant structures including microring resonators or Bragg gratings [9-11]. The group delay can be increased considerably around the resonance wavelengths. Although they can provide continuous delay tuning and compact sizes, they suffer from a limited operational bandwidth and are more sensitive to temperature variations. They also impose stricter requirement on fabrication in order to get uniform structures. Moreover, a low-loss, broadband OTTDL is increasingly appealing because of the limited optical power budget and the demand for broadband operations of the system. Therefore, it is more preferable to use the first method to implement long-range tunable delay lines in silicon photonics.

In this work, we propose and experimentally demonstrate 4-channel 5-bit OTTDLs on the silicon photonics platform. The delay is adjusted by the cascaded optical switches. The maximum delay reaches 511.5 ps with a 16.5 ps tuning step and the maximum delay error is less than ±1ps. By using wide ridge waveguides and Euler bends, we achieve low on-chip insertion loss ranging from 4.4 dB to 6 dB in the entire delay tuning range, corresponding to unit delay loss of 3 dB/ns.

2. Design structure

Figure 1(a) shows the schematic of the proposed delay line structure, incorporating four identical 5-bit OTTDLs. Each MZI switch element consists of two 2×2 multimode interferometers (MMIs) and two 300-μm-long waveguide arms integrated with a TiN microheater for phase tuning. VOAs are integrated in the delay waveguides to both suppress the crosstalk and calibrate the delay state. Time delay can be tuned from 0 to $(2^5\text{-}1)\Delta t$ with a resolution of Δt = 16.5 ps. Euler bends with an effective bending radius of about 5 μm and 2-μm-wide ridge waveguides are utilized to lower the optical transmission loss. Compared with a conventional bend of an equal radius, the Euler bend has lower loss and more compact size due to its varying bending radius [12-14]. Figure 1(b) shows the cross-section of the 2-μm-wide ridge waveguide. The wide width helps reduce the waveguide sidewall scattering loss. The ridge waveguide is transformed to a 500 nm wide channel waveguide in the bending sections. Figure 1(c) illustrates the cross-section of the p-i-n diode-based VOA. The highly doped P^{++} and N^{++} areas are 0.8 μm away from the ridge waveguide edge to lower the free-carrier absorption loss. Figure 1(d) shows the schematic of one stage OTTDL. The upper and lower arms have a differential length of $(2^{n\text{-}1}c\Delta t)/n_g$, where n is the stage number, c is the speed of light in vacuum, and n_g is the group index of the wide ridge waveguide. It should be noted that the length difference is given by the wide ridge waveguide, which helps improve the accuracy of the differential delay. The delay lines were designed for C-band and transverse electric (TE) polarization.

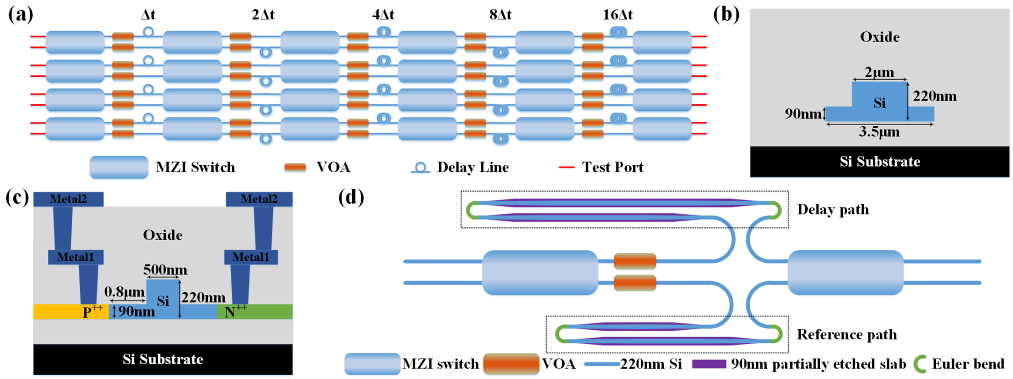

Fig. 1. (a) Schematic of the 4-channel OTTDLs chip. (b, c) Cross-sections of the (b) ridge waveguide and (c) VOA. (d) Schematic of one stage delay line.

This chip was fabricated on a silicon-on-insulator (SOI) platform with a silicon device layer thickness of 220 nm. Figure 2(a) depicts the microscope image of the fabricated chip. The chip footprint is 10 mm × 2.3 mm. Figure 2(b) shows the picture of the packaged chip. The chip was wire-bonded to a print circuit board (PCB). DC voltages were applied to the chip through I-PEX cables connected to the PCB. Two fiber arrays were edge-coupled to the input and output ports and fixed by ultraviolet-curable adhesive. Index matching oil of 1.40 refractive index was filled in the coupling gap to reduce the coupling loss and reflection. The coupling loss was measured to be around 1.9 dB/facet. A thermo-electric cooler (TEC) together with a thermistor was placed under the chip to monitor and stabilize the chip temperature. The chip was packaged in SJTU-Pinghu institute of intelligent optoelectronics (SPIOE).

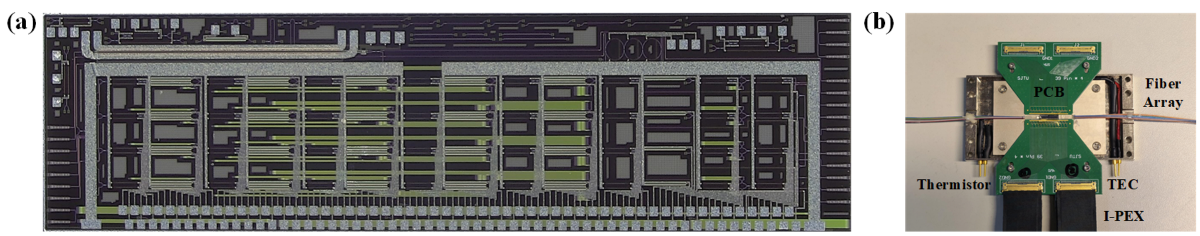

Fig. 2. (a) Microscope image of the chip. (b) Picture of the packaged chip.

3. Experimental results

We first characterized the performances of the key elements before the chip was packaged. The measured average propagation loss of the 2-μm-wide ridge waveguide is around 0.47 dB/cm. The 90° Euler bend loss is around 0.003 dB. The insertion loss and crosstalk of the MZI switch element is ~0.31 dB and -35 dB, respectively. The bar and cross states of the switch element have almost identical performances.

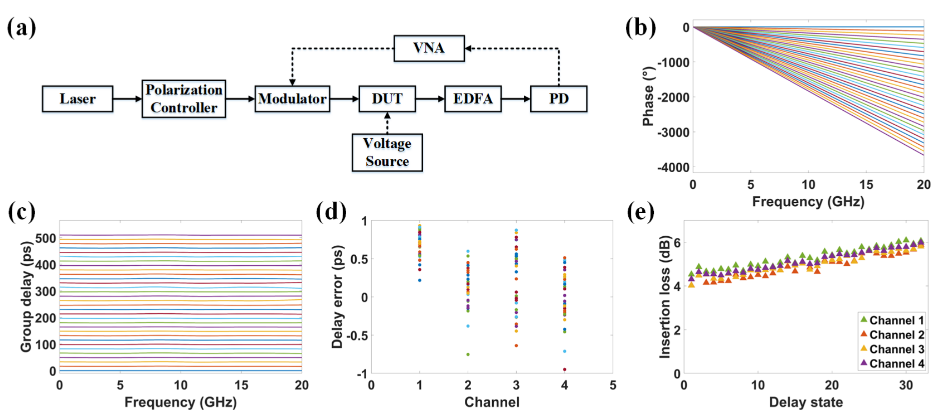

Fig. 3. (a) Experimental setup for delay measurement. The solid and dashed lines represent optical and electrical signals, respectively. DUT, device under test; EDFA, erbium doped fiber amplifier; PD, photodetector; VNA, vector network analyzer. (b) Phase and (c) group delay responses of the fourth-channel OTTDL. (d) Delay errors of the four-channel OTTDLs at the 18 GHz microwave frequency. (e) Insertion loss of all delay states for the four-channel OTTDLs.

We then measured the delay responses of all four OTTDLs. Figure 3(a) shows the experimental setup for the measurement of all delay states. The delay states of all four OTTDLs were calibrated by switching on the corresponding VOAs and maximizing the output power by adjusting the applied voltages on the MZI switches. An EDFA was used because of the relative high insertion loss of the modulator (~12 dB). Figures 3(b) and 3(c) show the phase and group delay responses, respectively. All the delay responses were normalized to the shortest path with the microwave frequency varying from 50 kHz to 20 GHz. Because of the identical structure of all four channels, only the delay responses of the fourth channel are presented here for demonstration. Group delay can be tuned from 0 to 511.5 ps with a step of 16.5 ps. Figure 3(d) presents the delay errors between the measurement and the target for all four OTTDLs at the 18 GHz microwave frequency. Among all the four OTTDLs, the maximum delay error is within ±1ps, resulted from the high fabrication tolerance of the wide ridge waveguides.

The insertion loss of the fourth-channel OTTDL varies from 4.4 dB to 6 dB when the delay is tuned from the minimum to the maximum, and therefore the unit delay loss is 3 dB/ns. Figure 3(e) shows the on-chip insertion loss for all four OTTDLs with 32 delay states each. The loss variation is below 0.67 dB among the four OTTDLs. We also characterized the switching time when the delay state was changed from one to the other. With a 150 Hz square-wave electrical signal applied to one of the MZI switches in the fourth-channel OTTDL, the rising and falling time latency between the electrical drive signal and the output optical signal was measured to be 51 μs and 66 μs, respectively.

4. Conclusions

We have experimentally demonstrated 4-channel 5-bit OTTDLs on the SOI platform. The delay loss varies from 4.4 dB to 6 dB as delay is tuned from 0 to 511.5 ps, corresponding to 3 dB/ns unit delay loss. The delay deviation among all four OTTDLs is within 1 ps. This chip features compact size, low insertion loss, and high delay accuracy, making it promising for application in broadband high-resolution phased array radar systems.

5. Funding

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